LM317M, NCV317MAB, NCV317MB

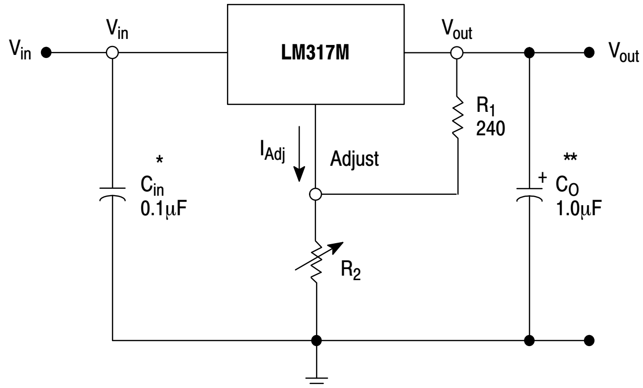
500 mA Adjustable Output, Positive Voltage Regulator

The LM317M is an adjustable three−terminal positive voltage regulator capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow−out proof.

The LM317M serves a wide variety of applications including local, on−card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317M can be used as a precision current regulator.

Features

- Output Current in Excess of 500 mA
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe−Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking Many Fixed Voltages
- Pb−Free Packages are Available
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

Figure 1. Simplified Application

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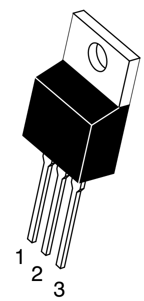
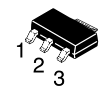
Heatsink surface connected to Pin 2

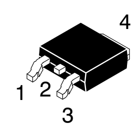
TO−220AB
T SUFFIX
CASE 221AB



SOT−223
ST SUFFIX
CASE 318E



DPAK
DT SUFFIX
CASE 369C



Heatsink Surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

PIN ASSIGNMENT	
1	Adjust
2	V_{out}
3	V_{in}

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 11 of this data sheet.

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March, 2008 − Rev. 17
Publication Order Number:
LM317M/D

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation (Package Limitation) (Note 1)			
Plastic Package, T Suffix, Case 221A			
T_A = 25°C	P_D	Internally Limited	
Thermal Resistance, Junction-to-Air	θ_{JA}	70	°C/W
Thermal Resistance, Junction-to-Case	θ_{JC}	5.0	°C/W
Plastic Package, DT Suffix, Case 369C			
T_A = 25°C	P_D	Internally Limited	
Thermal Resistance, Junction-to-Air	θ_{JA}	92	°C/W
Thermal Resistance, Junction-to-Case	θ_{JC}	5.0	°C/W
Plastic Package, ST Suffix, Case 318E			
T_A = 25°C	P_D	Internally Limited	
Thermal Resistance, Junction-to-Air	θ_{JA}	245	°C/W
Thermal Resistance, Junction-to-Case	θ_{JC}	15	°C/W
Operating Junction Temperature Range	T_J	−40 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Figure 25 provides thermal resistance versus PC board pad size.

ELECTRICAL CHARACTERISTICS ($V_I - V_O$ = 5.0 V; I_O = 0.1 A, T_J = T_{low} to T_{high} (Note 2), unless otherwise noted.)

Characteristics	Figure	Symbol	LM317M / LM317MB/NCV317MB Min	Typ	Max	Unit
Line Regulation (Note 3) (T_A = 25°C, 3.0 V ≤ $V_I - V_O$ ≤ 40 V)	3	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	4	Reg_{load}	 – –	 5.0 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	5	I_{Adj}	–	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ $V_I - V_O$ ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}	3, 4	ΔI_{Adj}	–	0.2	5.0	μA
Reference Voltage 3.0 V ≤ $V_I - V_O$ ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}	5	V_{ref}	1.20	1.25	1.30	V
Line Regulation 3.0 V ≤ V_I-V_O ≤ 40 V (Note 3)	3	Reg_{line}	–	0.02	0.07	%/V
Load Regulation 10 mA ≤ I_O ≤ 0.5 A (Note 3) V_O ≤ 5.0 V V_O ≥ 5.0 V	4	Reg_{load}	 – –	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	5	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O$ = 40 V)	5	I_{Lmin}	–	3.5	10	mA
Maximum Output Current $V_I - V_O$ ≤ 15 V, P_D ≤ P_{max} $V_I - V_O$ = 40 V, P_D ≤ P_{max}, T_A = 25°C	5	I_{max}	 0.5 0.15	 0.9 0.25	 – –	A
RMS Noise, % of V_O (T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz)	–	N	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 4) Without C_{Adj} C_{Adj} = 10 μF	6	RR	 – 66	 65 80	 – –	dB
Thermal Shutdown (Note 5)	–	–	–	180	–	°C
Long-Term Stability, T_J = T_{high} (Note 6) T_A= 25°C for End-point Measurements	5	S	–	0.3	1.0	%/1.0 kHrs.

2. T_{low} to T_{high} = 0° to +125°C for LM317M T_{low} to T_{high} = −40° to +125°C for LM317MB, NCV317MB.
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Thermal characteristics are not subject to production test.
6. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot-to-lot.

ELECTRICAL CHARACTERISTICS ($V_I - V_O$ = 5.0 V; I_O = 0.1 A, $T_J = T_{low}$ to T_{high} (Note 7), unless otherwise noted.)

Characteristics	Figure	Symbol	LM317MA / LM317MAB/NCV317MAB Min	Typ	Max	Unit
Line Regulation (Note 8) (T_A = 25°C, 3.0 V ≤ $V_I - V_O$ ≤ 40 V)	3	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 8) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	4	Reg_{load}	 – –	 5.0 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	5	I_{Adj}	–	50	100	µA
Adjustment Pin Current Change 2.5 V ≤ $V_I - V_O$ ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}	3, 4	ΔI_{Adj}	–	0.2	5.0	µA
Reference Voltage 3.0 V ≤ $V_I - V_O$ ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}	5	V_{ref}	1.225	1.250	1.275	V
Line Regulation (Note 8) 3.0 V ≤ V_I–V_O ≤ 40 V	3	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 8) 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	4	Reg_{load}	 – –	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	5	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O$ = 40 V)	5	I_{Lmin}	–	3.5	10	mA
Maximum Output Current $V_I - V_O$ ≤ 15 V, P_D ≤ P_{max} $V_I - V_O$ = 40 V, P_D ≤ P_{max}, T_A = 25°C	5	I_{max}	 0.5 0.15	 0.9 0.25	 – –	A
RMS Noise, % of V_O (T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz)	–	N	–	–	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 9) Without C_{Adj} C_{Adj} = 10 µF	6	RR	 – 66	 65 80	 – –	dB
Thermal Shutdown (Note 10)	–	–	–	180	–	°C
Long-Term Stability, $T_J = T_{high}$ (Note 11) T_A= 25°C for End-point Measurements	5	S	–	0.3	1.0	%/1.0 kHrs.

7. T_{low} to T_{high} = 0° to +125°C for LM317MA T_{low} to T_{high} = −40° to +125°C for LM317MAB, NCV317MAB.
8. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
9. C_{Adj}, when used, is connected between the adjustment pin and ground.
10. Thermal characteristics are not subject to production test.
11. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot-to-lot.

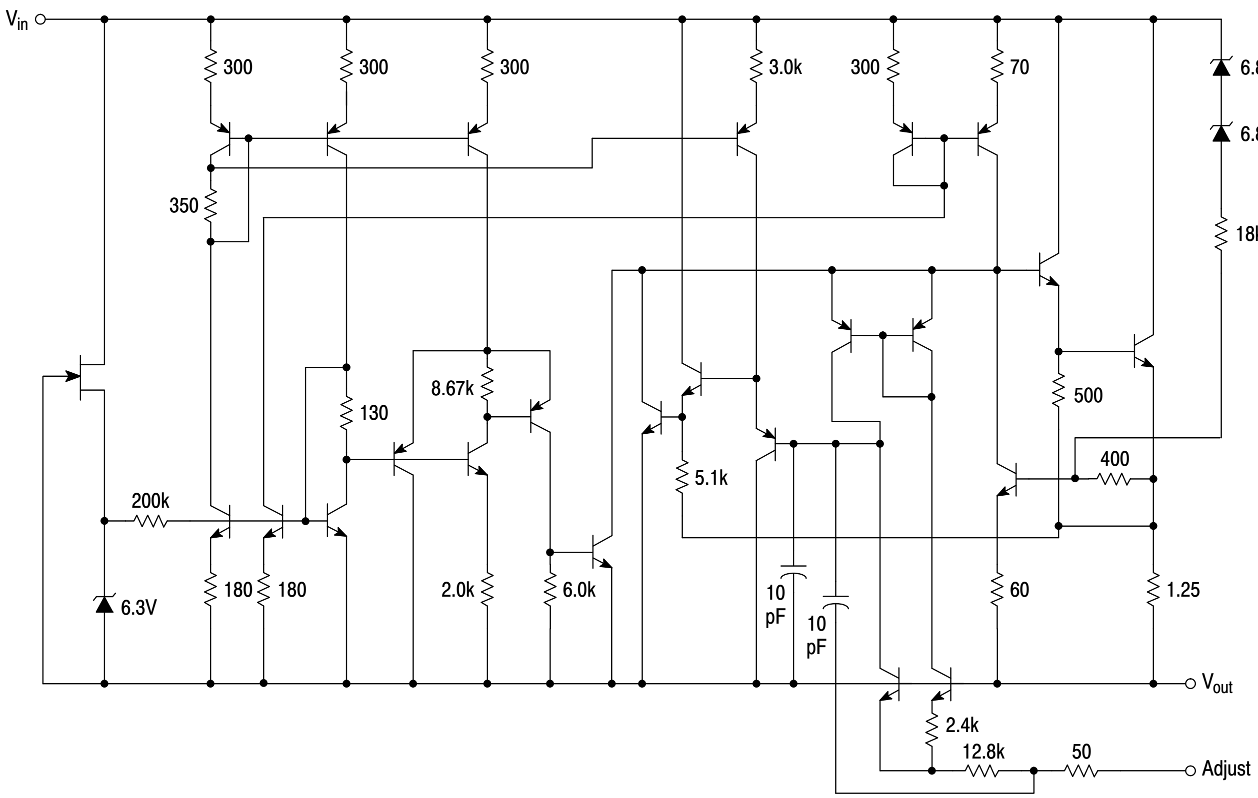


Figure 2. Representative Schematic Diagram

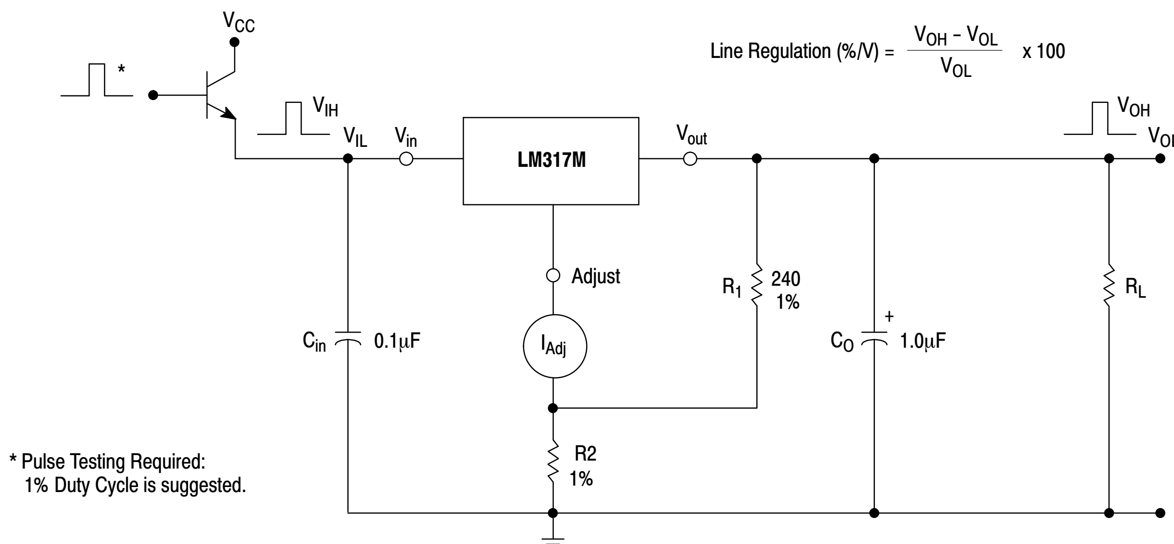
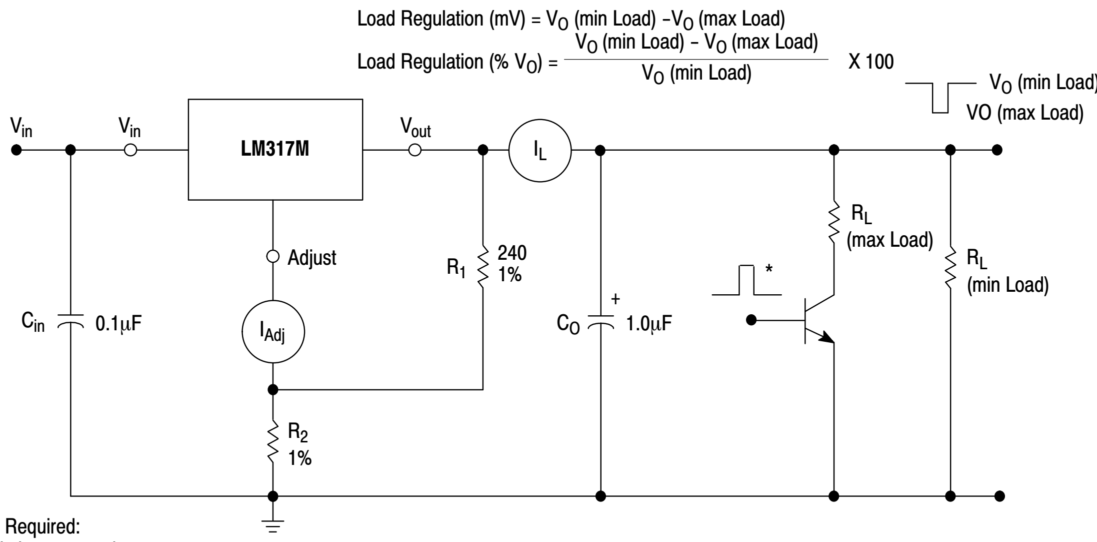
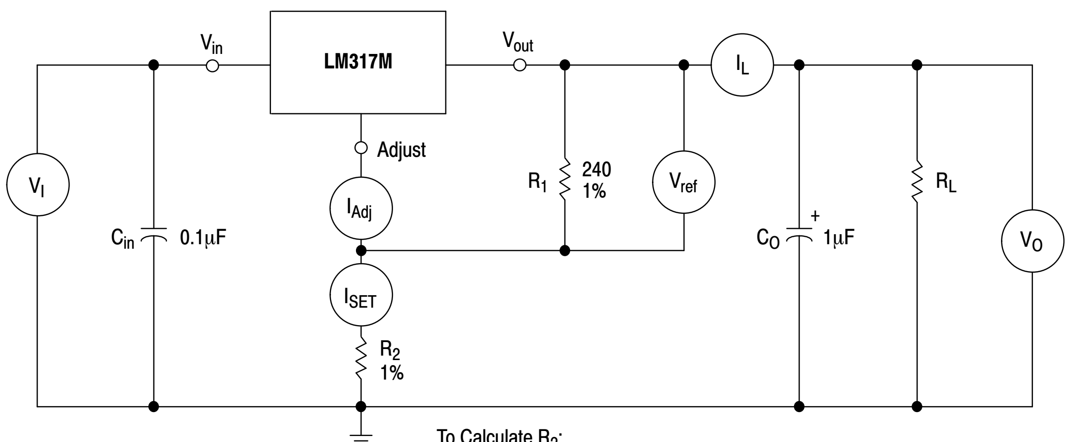


Figure 3. Line Regulation and ΔI_{Adj}/Line Test Circuit



* Pulse Testing Required:
1% Duty Cycle is suggested.

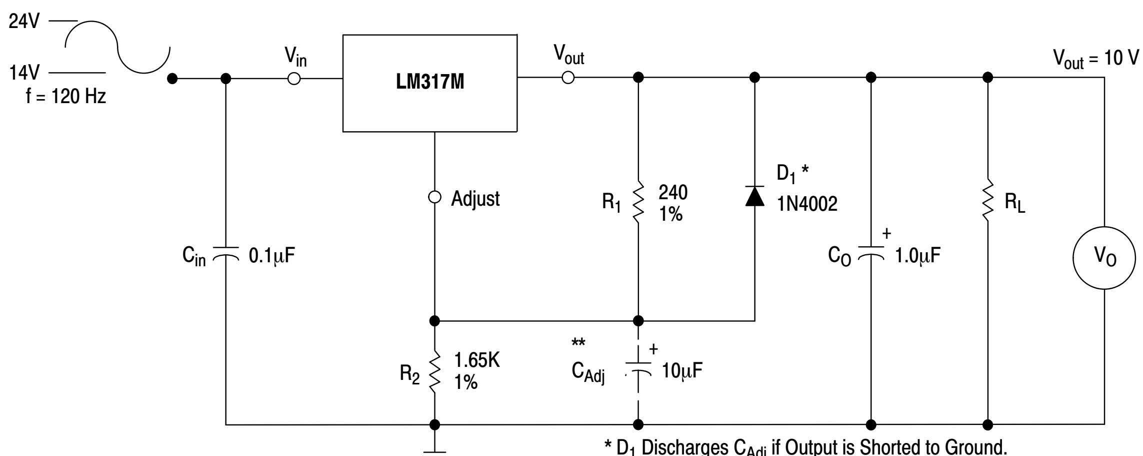
Figure 4. Load Regulation and ΔI_{Adj}/Load Test Circuit



*Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 5. Standard Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.
**C_{Adj} provides an AC ground to the adjust pin.

Figure 6. Ripple Rejection Test Circuit

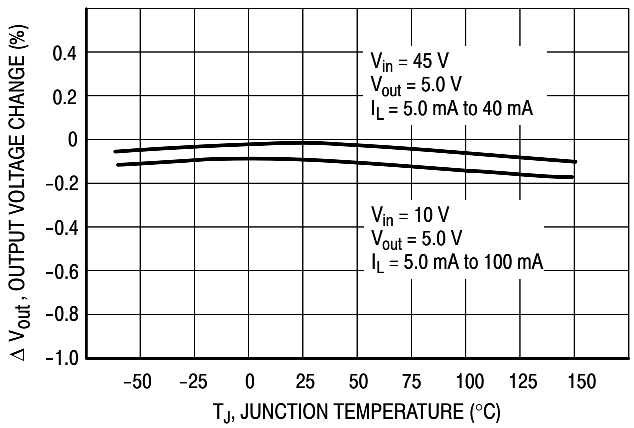


Figure 7. Load Regulation

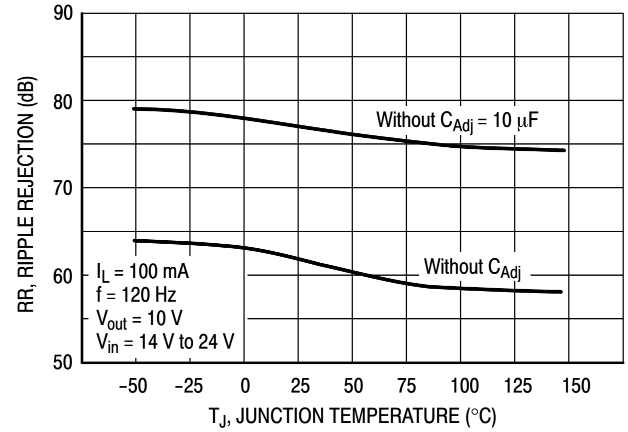


Figure 8. Ripple Rejection

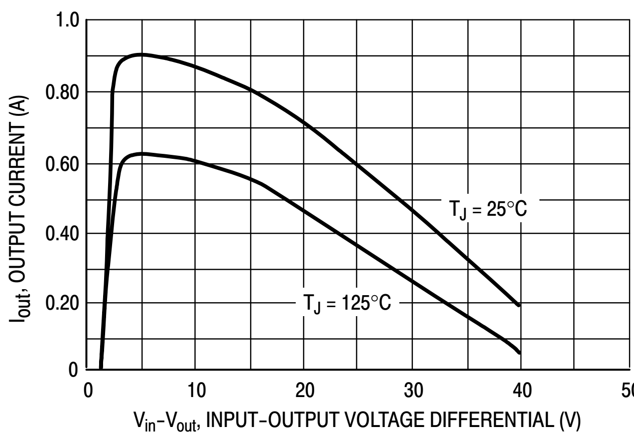


Figure 9. Current Limit

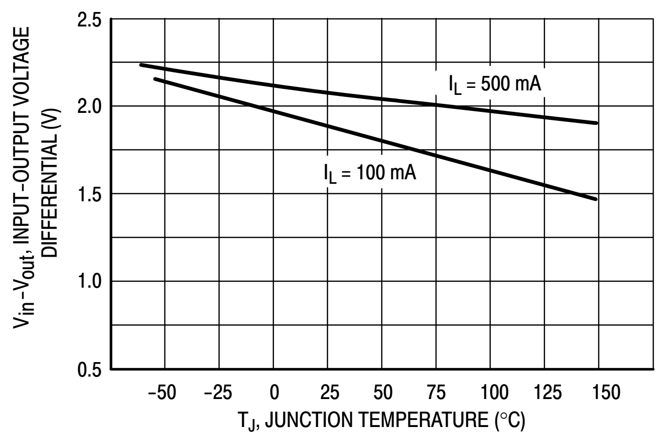


Figure 10. Dropout Voltage

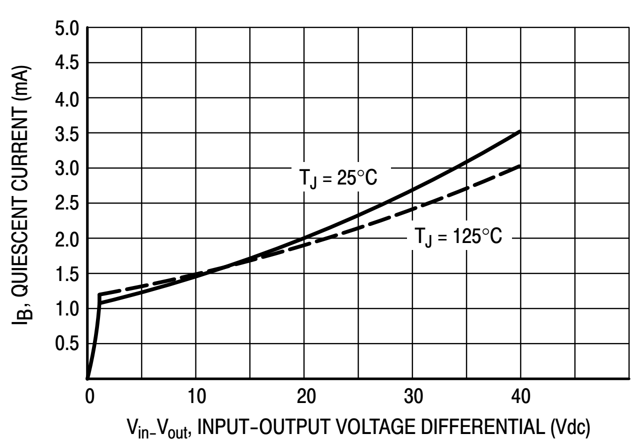


Figure 11. Minimum Operating Current

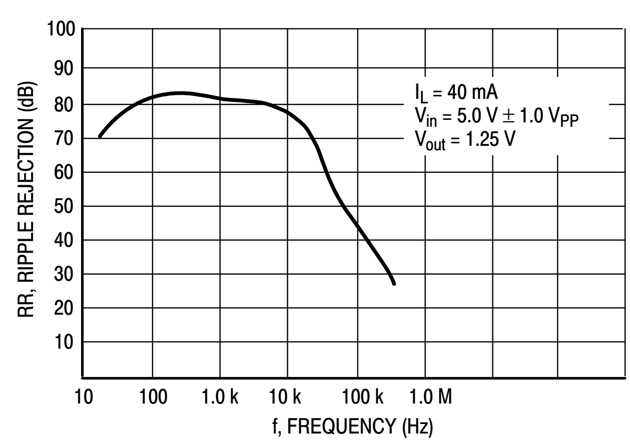


Figure 12. Ripple Rejection versus Frequency

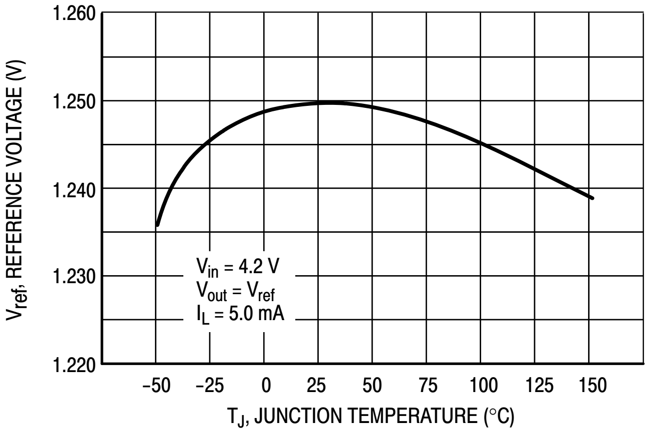


Figure 13. Temperature Stability

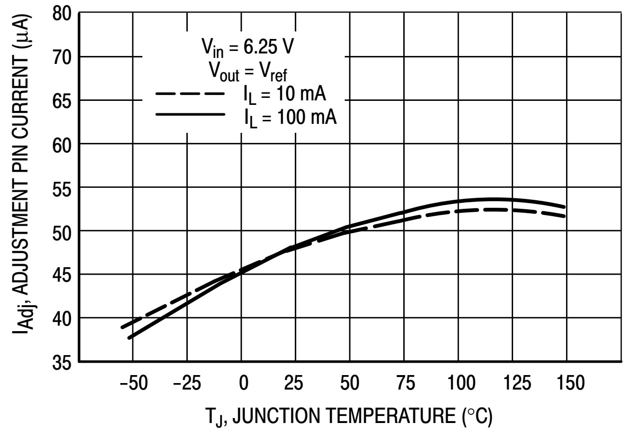


Figure 14. Adjustment Pin Current

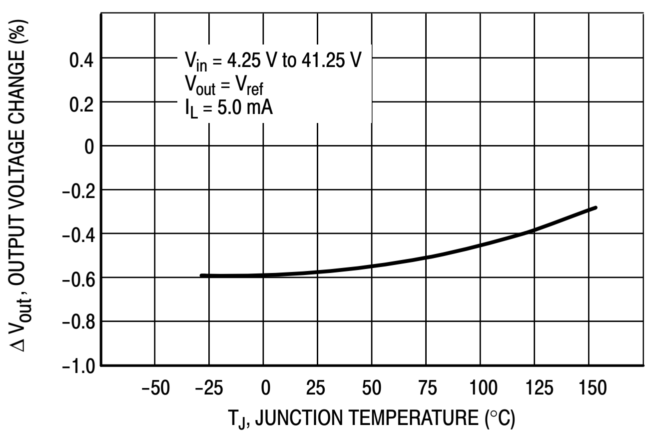


Figure 15. Line Regulation

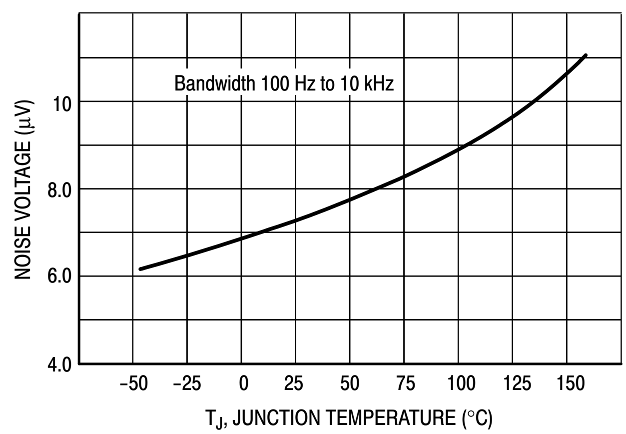


Figure 16. Output Noise

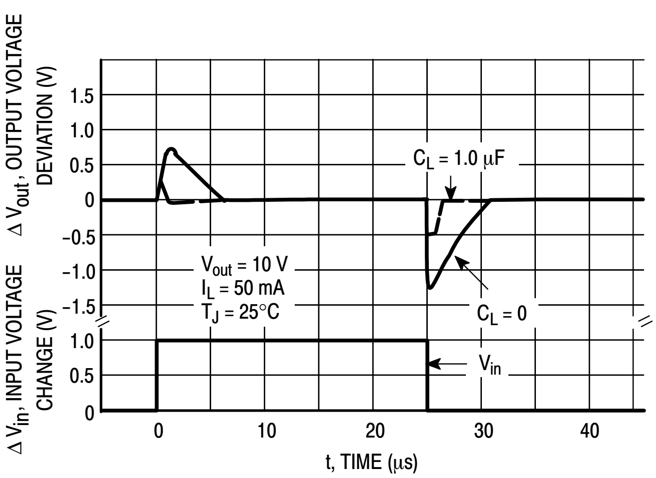


Figure 17. Line Transient Response

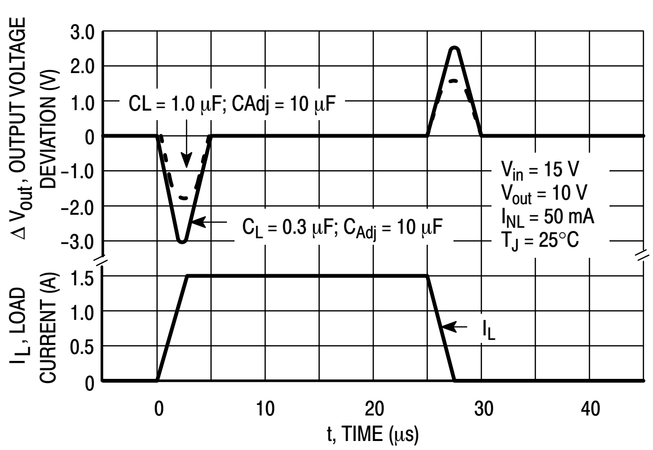


Figure 18. Load Transient Response

APPLICATIONS INFORMATION

Basic Circuit Operation

The LM317M is a three-terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 19), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since the current from the terminal (I_{Adj}) represents an error term in the equation, the LM317M was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

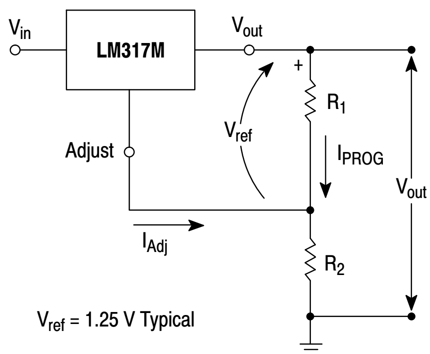


Figure 19. Basic Circuit Configuration

Load Regulation

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 20 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25$ μF, $C_{Adj} > 5.0$ μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

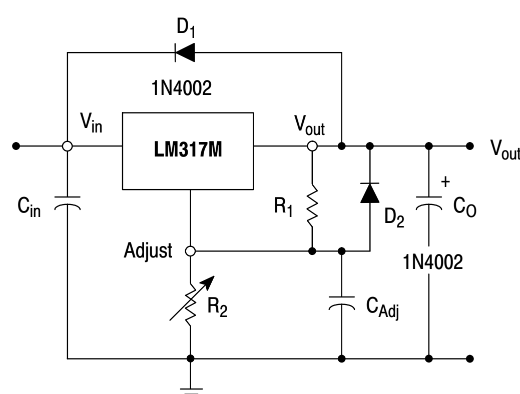


Figure 20. Voltage Regulator with Protection Diodes

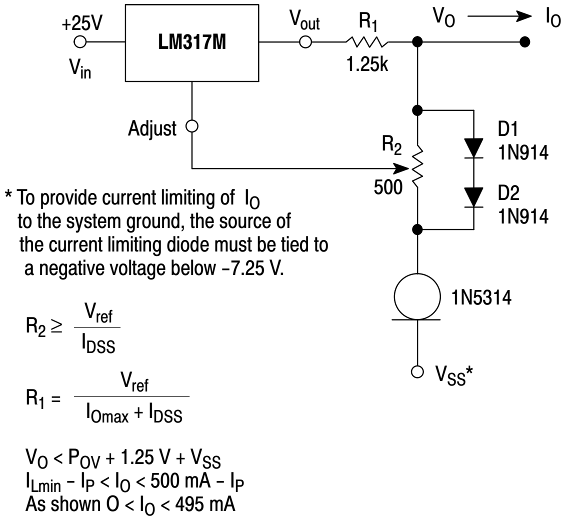


Figure 21. Adjustable Current Limiter

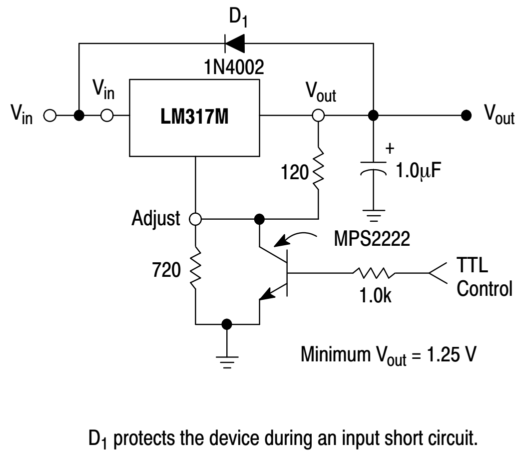


Figure 22. 5 V Electronic Shutdown Regulator

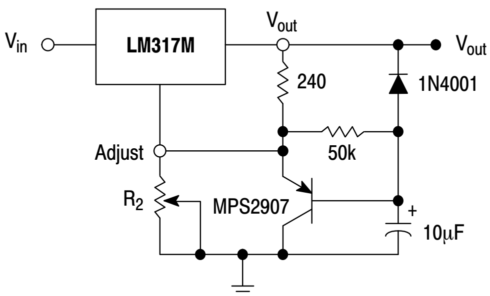


Figure 23. Slow Turn−On Regulator

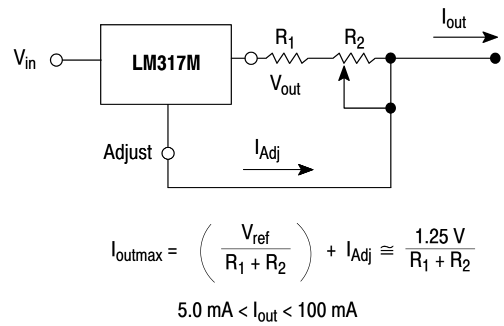


Figure 24. Current Regulator

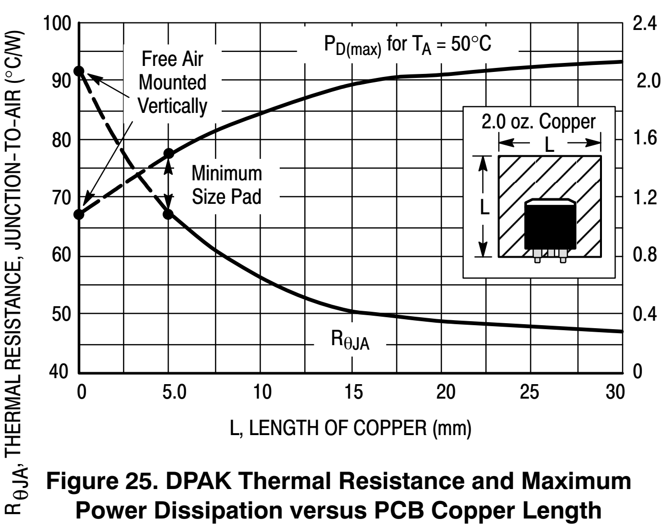


Figure 25. DPAK Thermal Resistance and Maximum Power Dissipation versus PCB Copper Length

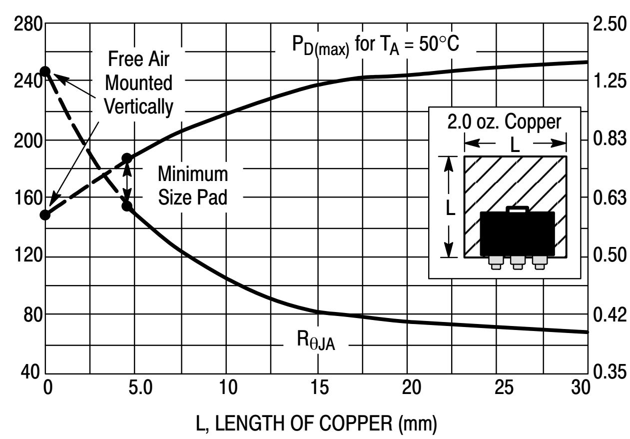


Figure 26. SOT−223 Thermal Resistance and Maximum Power Dissipation versus PCB Copper Length

ORDERING INFORMATION

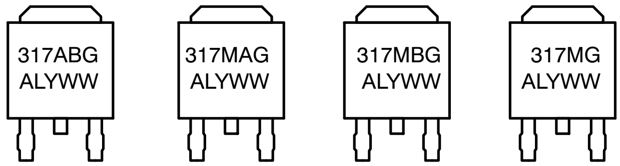
Device	Output Voltage Tolerance	Operating Temperature Range	Package	Shipping†
LM317MABDT	2%	T_J = −40°C to 125°C	DPAK	75 Units / Rail
LM317MABDTG			DPAK (Pb−Free)	75 Units / Rail
LM317MABDTRK			DPAK	2500 / Tape & Reel
LM317MABDTRKG			DPAK (Pb−Free)	2500 / Tape & Reel
LM317MABT			TO−220	50 Units / Rail
LM317MABTG			TO−220 (Pb−Free)	50 Units / Rail
NCV317MABDTRKG*			DPAK (Pb−Free)	2500 / Tape & Reel
LM317MADTRK		T_J = 0°C to 125°C	DPAK	2500 / Tape & Reel
LM317MADTRKG			DPAK (Pb−Free)	2500 / Tape & Reel
LM317MBDT	4%	T_J = −40°C to 125°C	DPAK	75 Units / Rail
LM317MBDTG			DPAK (Pb−Free)	75 Units / Rail
LM317MBDTRK			DPAK	2500 / Tape & Reel
LM317MBDTRKG			DPAK (Pb−Free)	2500 / Tape & Reel
LM317MBSTT3			SOT−223	4000 / Tape & Reel
LM317MBSTT3G			SOT−223 (Pb−Free)	4000 / Tape & Reel
LM317MBT			TO−220	50 Units / Rail
LM317MBTG			TO−220 (Pb−Free)	50 Units / Rail
NCV317MBDTG*			DPAK (Pb−Free)	75 Units / Rail
NCV317MBDTRK*			DPAK	2500 / Tape & Reel
NCV317MBDTRKG*			DPAK (Pb−Free)	2500 / Tape & Reel
LM317MDT		T_J = 0°C to 125°C	DPAK	75 Units / Rail
LM317MDTG			DPAK (Pb−Free)	75 Units / Rail
LM317MDTRK			DPAK	2500 / Tape & Reel
LM317MDTRKG			DPAK (Pb−Free)	2500 / Tape & Reel
LM317MSTT3			SOT−223	4000 / Tape & Reel
LM317MSTT3G			SOT−223 (Pb−Free)	4000 / Tape & Reel
LM317MT			TO−220	50 Units / Rail
LM317MTG			TO−220 (Pb−Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

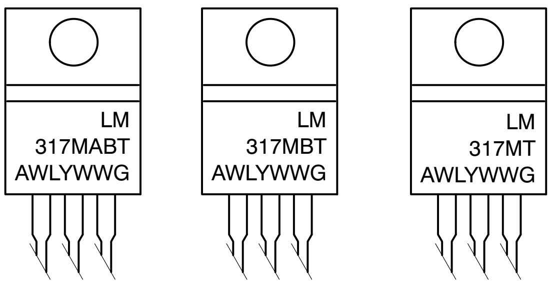
* NCV devices: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and control change.

MARKING DIAGRAMS

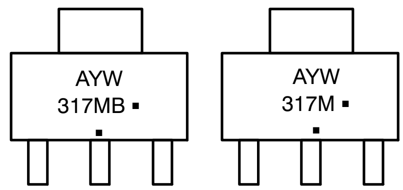
DPAK
DT SUFFIX
CASE 369C



TO−220
T SUFFIX
CASE 221A



SOT−223
ST SUFFIX
CASE 318E

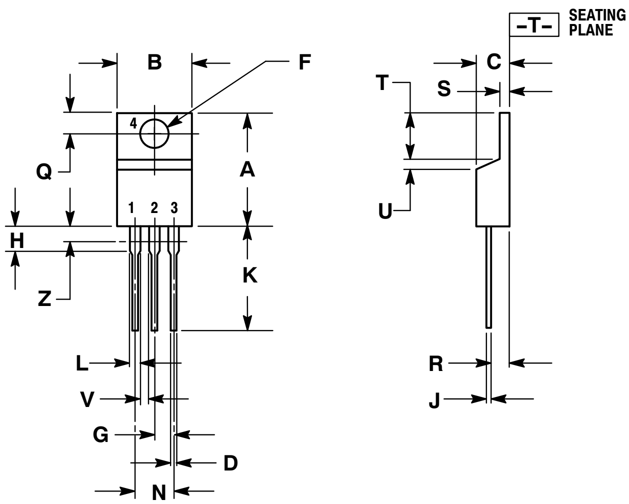


A	= Assembly Location
L, WL	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PACKAGE DIMENSIONS

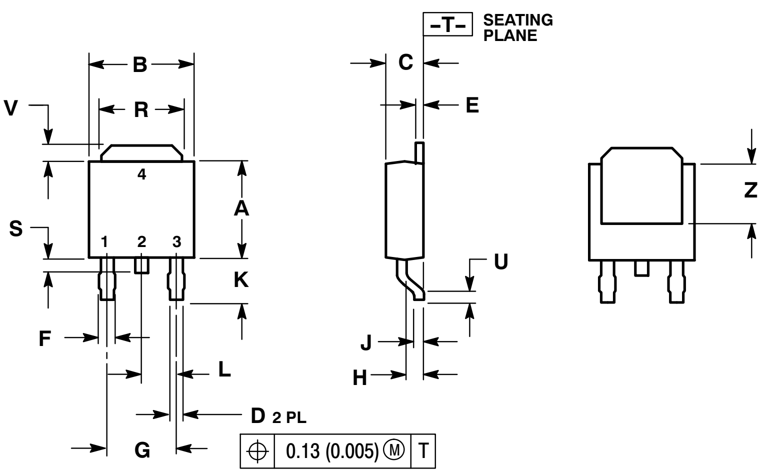
TO−220, SINGLE GAUGE
T SUFFIX
PLASTIC PACKAGE
CASE 221AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.055	0.508	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

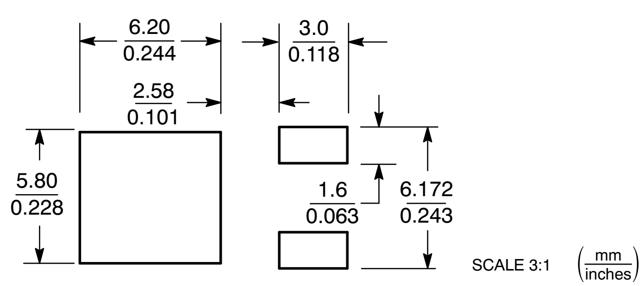
DPAK
DT SUFFIX
PLASTIC PACKAGE
CASE 369C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

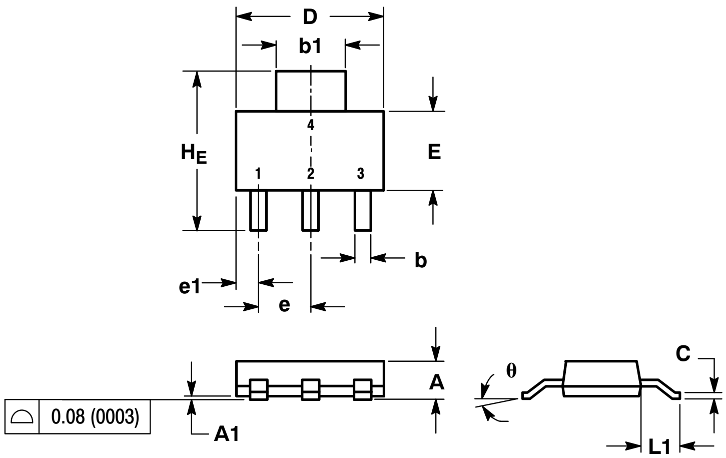
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

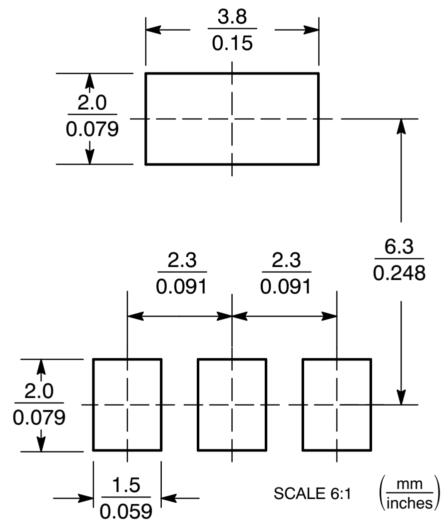
SOT−223 (TO−261)
ST SUFFIX
PLASTIC PACKAGE
CASE 318E−04
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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